

Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

C1 1-33 (cancelled)

34. (new): A data processing system, comprising:

a processor;

a main memory;

a multi-ported memory in communication with the processor and the main memory, the multi-ported memory having a storage capacity of about 4 kilobytes or greater; and

wherein the system is configured to receive a request to write information to a memory location, wherein the information has an information type equal to data or control information, and wherein the system is further configured to determine a memory destination between the main memory or the multi-ported memory based on the information type.

35. (new): The system of claim 34, further comprising an operating system configured to determine the memory destination based on the information type.

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36. (new): The system of claim 34, wherein the system further includes:

a peripheral device; and

a peripheral device controller, wherein the controller is configured to determine the memory destination based on the information type.

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37. (new): The system of claim 34, wherein the multi-ported memory is included in a memory controller.

38. (new): The system of claim 34, wherein the multi-ported memory is dual-ported.

39. (new): The system of claim 34, wherein the multi-ported memory and memory controller are integrated into a single chip.

40. (new): The system of claim 34, wherein the multi-ported memory includes memory chosen from the group consisting of static random access memory and dynamic random access memory.

41. (new): The system of claim 34, wherein the multi-ported memory stores reservation bits mapped to blocks of general-purpose memory in the multi-ported memory.

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42. (new): The system of claim 34, wherein virtual addresses within multi-ported memory are mapped to physical addresses with smart addressing.

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43. (new): The system of claim 34, further including:
a memory controller in communication with the main memory and the multi-ported memory; and
a peripheral device in communication with the memory controller via an input/output bus.

44. (new): The system of claim 34, wherein for information with an information type equal to control information, the system is configured to determine the memory destination to be the multi-ported memory and not the main memory.

45. (new): A method comprising:
receiving a request to write information to a memory location;
determining an information type equal to data or control information for the information; and
determining a memory destination between a main memory and a multi-ported memory based on the information type, the multi-ported memory having a storage capacity of about 4 kilobytes or greater.

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46. (new): The method of claim 45, further comprising:
writing the information to the memory destination based on
the determining the memory destination.

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47. (new): The method of claim 45, wherein determining the
memory destination between the main memory and the multi-ported
memory based on the information type comprises determining the
memory destination to be the multi-ported memory for the
information type equal to control information.

48. (new): An article comprising a computer-readable medium
which stores computer-executable instructions, the instructions
causing one or more machines to perform operations comprising:

receiving a request to write information to a memory
location;

determining an information type equal to data or control
information for the information; and

determining a memory destination between a main memory and
a multi-ported memory based on the information type, the multi-
ported memory having a storage capacity of about 4 kilobytes or
greater.

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49. (new): The article of claim 48, further comprising:
writing the information to the memory destination based on
the determining the memory destination.

50. (new): The article of claim 48, wherein determining the
memory destination between the main memory and the multi-ported
memory based on the information type comprises determining the
memory destination to be the multi-ported memory for the
information type equal to control information.
